Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-3 (Cancelled).

4. (Currently Amended) A digital synchronous circuit, comprising:

a clock generating circuit for outputting a plurality of clock signals having same frequency and different phases;

a plurality of first latch circuits for taking in an input data signal according to corresponding ones of said plurality of clock signals;

a control circuit for outputting a control signal after a prescribed period of time according to a change in said input data signal; and

a plurality of second latch circuits for taking in and holding outputs of said plurality of first latch circuits, respectively, according to said control signal, wherein said control circuit includes

a pulse generating circuit for generating a pulse signal according to a change in said input data signal, and

a delay circuit for receiving said pulse signal and entering a meta-stable state for at least part of, but not more than, said prescribed period time to cause delay for said prescribed period of time, wherein

the delay circuit comprises a third latch circuit for receiving said pulse signal at a data input node and a clock input node, and

said third latch circuit has a first output node for outputting a signal of an equal polarity to said data input signal and a second output node for outputting an inverted output of said signal output from said first output node.

5. (Previously Presented) A digital synchronous circuit, comprising:

a clock generating circuit for outputting a plurality of clock signals having same frequency and different phases;

a plurality of first latch circuits for taking in an input data signal according to corresponding ones of said plurality of clock signals;

a control circuit for outputting a control signal after a prescribed period of time according to a change in said input data signal;

a plurality of second latch circuits for taking in and holding outputs of said plurality of first latch circuits, respectively, according to said control signal, wherein said control circuit includes

a first pulse generating circuit for generating a first pulse signal according to a change in said input data signal,

a third latch circuit for receiving said first pulse signal at a data input node and a clock input node,

a level determination circuit for outputting a detection signal when potential of an output signal from said third latch circuit has crossed a reference potential, and

a second pulse generating circuit for generating a second pulse signal according to a change in potential of said detection signal and outputting said second pulse signal as said control signal.

6. (Original) The digital synchronous circuit according to claim 5, wherein said third latch circuit has same circuit configuration as said first latch circuit.

7. (Original) The digital synchronous circuit according to claim 5, wherein

said third latch circuit has a first output node for outputting a signal of an equal polarity to said data input signal and a second output node for outputting an inverted output of said signal output from said first output node, and

said control circuit further includes a field-effect transistor connected between said first output node and said second output node for receiving said first pulse signal at a gate.

8. (Original) The digital synchronous circuit according to claim 5, wherein

said third latch circuit has a first output node for outputting a signal of an equal polarity to said data input signal and a second output node for outputting an inverted output of said signal output from said first output node, and wherein

said level determination circuit includes

a first level determination unit for determining whether potential of said first output node has reached a prescribed potential level,

a second level determination unit for determining whether potential of said second output node has reached said prescribed potential level, and

a first logic gate circuit for outputting said detection signal according to outputs from said first and second level determination units.

9. (Original) The digital synchronous circuit according to claim 8, wherein said first level determination unit includes a first differential input comparator for receiving a potential level of said first output node and said prescribed potential level, and

said second level determination unit includes a second differential input comparator for receiving a potential level of said second output node and said prescribed potential level.

10. (Original) The digital synchronous circuit according to claim 8, wherein said first and second level determination units have second and third logic gate circuits, respectively, whose threshold voltages each is said prescribed potential level.

11. (Original) The digital synchronous circuit according to claim 8, wherein said level determination circuit includes

a first level determination unit for determining whether potential of an output signal from said third latch circuit has crossed a first potential level,

a second level determination unit for determining whether potential of an output signal from said third latch circuit has crossed a second potential level lower than said first potential level, and

a first logic gate circuit for outputting said detection signal according to outputs from said first and second level determination units.

12. (Original) The digital synchronous circuit according to claim 11, wherein said first level determination unit includes a first differential input comparator for receiving a potential level of an output node of said third latch circuit and said first potential level, and

said second level determination unit includes a second differential input comparator for receiving the potential level of said output node and said second potential level.

13. (Original) The digital synchronous circuit according to claim 11, wherein

said first level determination unit includes a second logic gate circuit whose threshold voltage is said first potential level,

said second level determination unit includes a third logic gate circuit whose threshold voltage is said second potential level,

said first potential level is an intermediate potential between a potential that is a half of a power-supply potential and said power-supply potential, and

said second potential level is an intermediate potential between the potential that is a half of said power-supply potential and a ground potential.

14. (Previously Presented) The digital synchronous circuit according to claim 1, further comprising:

a clock phase determination circuit for monitoring data held in said plurality of second latch circuits to determine an internal clock signal matching in phase with said input data signal from said plurality of clock signals; and

a selector for selecting an internal latch clock signal for suitably sampling said input data signal from said plurality of clock signals according to an output from said clock phase determination circuit and outputting selected said internal latch clock signal.

15. (Previously Presented) The digital synchronous circuit according to claim 8, further comprising:

a clock phase determination circuit for monitoring data held in said plurality of second latch circuits to determine an internal clock signal matching in phase with said input data signal from said plurality of clock signals; and

a selector for selecting an internal latch clock signal for suitably sampling said input data signal from said plurality of clock signals according to an output from said clock phase determination circuit and outputting selected said internal latch clock signal.

16. (Cancelled)

17. (Cancelled)

18. (Currently Amended) The digital synchronous circuit according to claim 4 ~~claim 17~~, wherein said control circuit further includes a field-effect transistor connected between said first output node and said second output node for receiving said pulse signal at its gate.

~~19.~~ 14 (Currently Amended) The digital synchronous circuit according to claim ~~4~~ 1 ~~claim 16~~, further comprising a level determination circuit for detecting when potential said third latch circuit is not in the meta-stable state and outputting a detection signal.

~~20.~~ 15 (Previously Presented) The digital synchronous circuit according to claim ~~19~~ 14, wherein said pulse generating circuit is a first pulse generating circuit, said delay circuit further comprising a second pulse generating circuit for generating a second pulse signal according to said detection signal and outputting said second pulse signal as said control signal.